AMENDMENTS TO THE CLAIMS

Please add or amend the claims to read as follows:

1. (Currently amended) A method for forming a non-volatile memory device, the method comprising:

forming an oxide-nitride-oxide (ONO) layer over a portion of a substrate, said ONO layer comprising a bottom oxide layer, a top oxide layer and a nitride layer intermediate said bottom and top oxide layers; and

managing movement of at least one of electrons and holes from said substrate towards said ONO layer by ~~controlling~~ selecting a thickness of at least one of said bottom oxide layer, said nitride layer and said top oxide layer, wherein said top oxide layer is at least 1.5 times thicker than said bottom oxide layer.

2. (Original) The method according to claim 1 wherein said managing comprises forming a thickness of said top oxide layer in a range of approximately 6-20 nm.

3. (Original) The method according to claim 1 wherein said managing comprises forming a thickness of said nitride layer in a range of approximately 1-2 nm.

4. (Original) The method according to claim 1 wherein said managing comprises forming a thickness of said bottom oxide layer in a range of approximately 4-5 nm.

5. (Original) The method according to claim 1 wherein said managing comprises forming said top oxide layer to be at least three times thicker than said nitride layer.

6. (Original) The method according to claim 1 wherein said managing comprises forming

[illegible]

[illegible]

said top oxide layer to be at least 1.5 times thicker than said bottom oxide layer.

8. (Original) The method according to claim 1 wherein said managing comprises forming said top oxide layer to be approximately 1.5-4 times thicker than said bottom oxide layer.

9. (Original) The method according to claim 1 wherein said managing comprises forming said top oxide layer to be at least half of an overall thickness of said ONO layer.

10. (Currently amended) A method for forming a non-volatile memory device, the method comprising:

forming an oxide-nitride-oxide (ONO) layer over a portion of a substrate, said ONO layer comprising a bottom oxide layer, a top oxide layer and a nitride layer intermediate said bottom and top oxide layers;

forming a gate over at least a portion of said ONO layer; and

decreasing a capacitance between said gate and said nitride layer by ~~controlling~~ selecting a thickness of at least one of said bottom oxide layer, said nitride layer and said top oxide layer, wherein said top oxide layer is at least 1.5 times thicker than said bottom oxide layer.

11. (Currently amended) A method for forming a non-volatile memory device, the method comprising:

forming an oxide-nitride-oxide (ONO) layer over a portion of a substrate, said ONO layer comprising a bottom oxide layer, a top oxide layer and a nitride layer intermediate said bottom and top oxide layers;

forming a gate over at least a portion of said ONO layer; and

increasing a threshold voltage of said non-volatile memory device per number of electrons injectable into said nitride layer by ~~controlling~~ selecting a thickness of at least one of

is at least 1.5 times thicker than said bottom oxide layer.

12. (Currently amended) A method for forming a non-volatile memory device, the method comprising:

forming an oxide-nitride-oxide (ONO) layer over a portion of a substrate, said ONO layer comprising a bottom oxide layer, a top oxide layer and a nitride layer intermediate said bottom and top oxide layers;

forming a gate over at least a portion of said ONO layer; and

decreasing a threshold voltage of said non-volatile memory device per number of holes injectable into said nitride layer by ~~controlling~~ selecting a thickness of at least one of said bottom oxide layer, said nitride layer and said top oxide layer, wherein said top oxide layer is at least 1.5 times thicker than said bottom oxide layer.

13. (Currently amended) A method for forming a non-volatile memory device, the method comprising:

forming an oxide-nitride-oxide (ONO) layer over a portion of a substrate, said ONO layer comprising a bottom oxide layer, a top oxide layer and a nitride layer intermediate said bottom and top oxide layers;

forming a gate over at least a portion of said ONO layer; and

narrowing a distribution of electrons injectable into said nitride layer by ~~controlling~~ selecting a thickness of at least one of said bottom oxide layer, said nitride layer and said top oxide layer, wherein said top oxide layer is at least 1.5 times thicker than said bottom oxide layer.

14. (Currently amended) A method for forming a non-volatile memory device, the method

forming an oxide-nitride-oxide (ONO) layer over a portion of a substrate, said ONO layer comprising a bottom oxide layer, a top oxide layer and a nitride layer intermediate said bottom and top oxide layers;

forming a gate over at least a portion of said ONO layer; and

improving a matching of electrons and holes injectable into said nitride layer by ~~controlling~~ selecting a thickness of at least one of said bottom oxide layer, said nitride layer and said top oxide layer, wherein said top oxide layer is at least 1.5 times thicker than said bottom oxide layer.

15. (Currently amended) A method for forming a non-volatile memory device, the method comprising:

forming an oxide-nitride-oxide (ONO) layer over a portion of a substrate, said ONO layer comprising a bottom oxide layer, a top oxide layer and a nitride layer intermediate said bottom and top oxide layers;

forming a gate over at least a portion of said ONO layer; and

enabling a reduction of operational current in said substrate by ~~controlling~~ selecting a thickness of at least one of said bottom oxide layer, said nitride layer and said top oxide layer, wherein said top oxide layer is at least 1.5 times thicker than said bottom oxide layer.

16. (Currently amended) A method for operating a non-volatile memory device, the method comprising:

providing an oxide-nitride-oxide (ONO) layer over a portion of a substrate, said ONO layer comprising a bottom oxide layer, a top oxide layer and a nitride layer intermediate said

applying operating voltages to said non-volatile memory device; and

controlling said operating voltages by ~~controlling~~ selecting a thickness of at least one of said bottom oxide layer, said nitride layer and said top oxide layer, wherein said top oxide layer is at least 1.5 times thicker than said bottom oxide layer.

17. (Withdrawn)

18. (Withdrawn)

19. (Withdrawn)

20. (Withdrawn)

21. (Withdrawn)

22. (Withdrawn)

23. (Withdrawn)

24. (Withdrawn)